Marvell® Alaska® C 88X7121P

Dual 400G, Quad 200G, Octal 100G, 16 port 50G/25G/10G/1G Ethernet
Transceiver with 256-bit MACsec Encryption and Class C PTP Timestamping

Overview

The Marvell® Alaska® C 88X7121P is a fully integrated single chip Ethernet transceiver that performs IEEE 802.1AE MACsec encryption with 256-bit key and IEEE 1588v2 PTP timestamping functionality for two ports of 400 GbE, four ports of 200 GbE, 8 ports of 100 GbE, 16 ports of 50 GbE, 25 GbE, 10 GbE, and 1 GbE. The device supports full-duplex transmission at all supported speeds, over a variety of media including optics, passive direct attach cables, and copper backplanes.

The device also supports a variety of gearboxing modes to translate between NRZ and PAM4 modes for 50 GbE and 100 GbE, with the necessary FEC termination and regeneration required to translate between NRZ and PAM4 operation.

The PTP timestamping functionality in the device provides timing accuracy that meets the requirements of Class C profile, enabling high precision timing recovery required for wireless and carrier applications. The device provides recovered clock for SyncE applications, with flexible clock source selection.
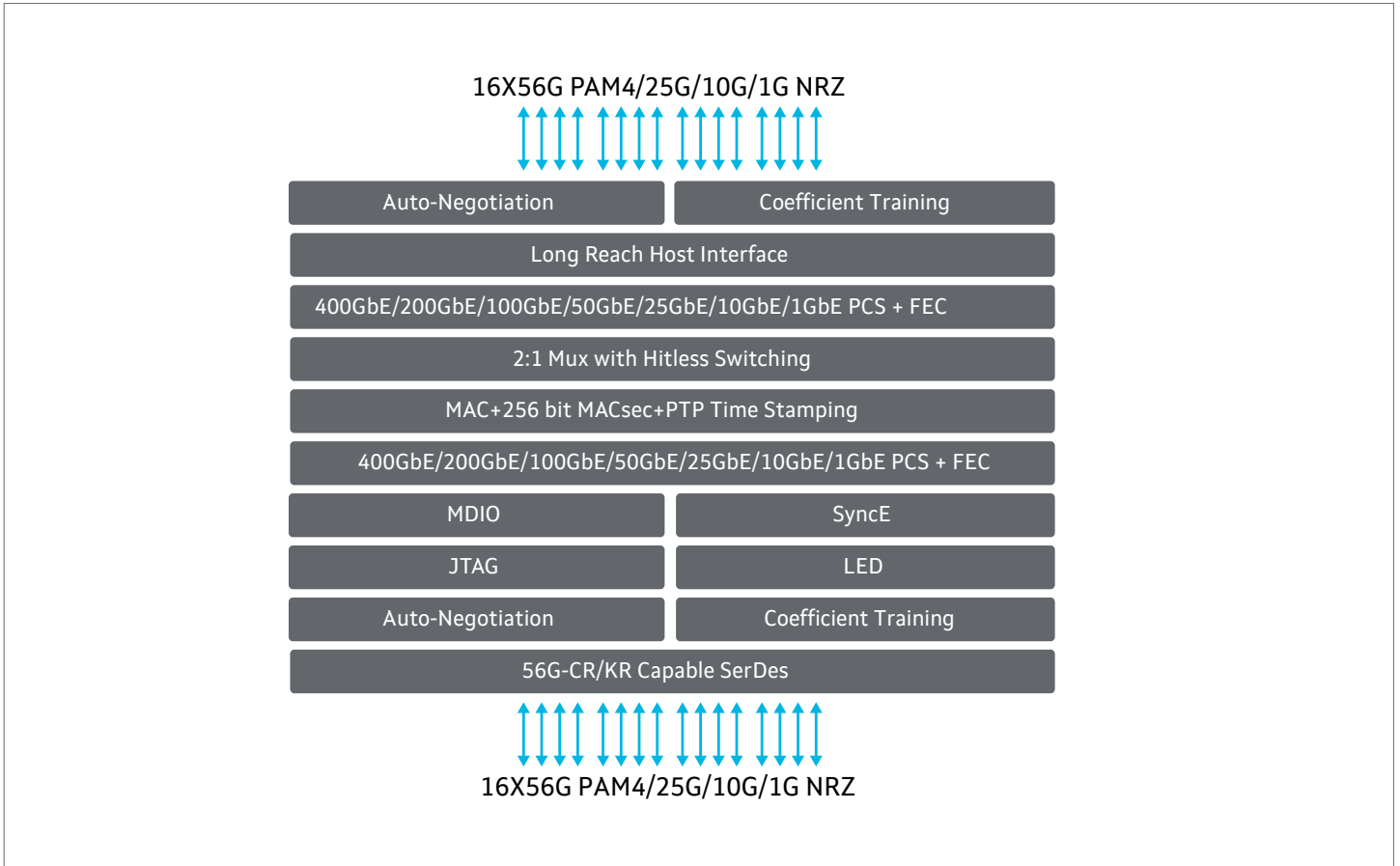
The 88X7121P integrates Long Reach dual mode (PAM4 and NRZ) SerDes, fully compliant to the IEEE electrical specifications for transmission over passive direct attach cables and copper backplanes. The device supports FEC generation and termination capabilities for all FEC types defined by IEEE 802.3cd, 802.3by, 802.3bj, 802.3ba, 802.3ap and the 25 Gigabit Ethernet Consortium for 400 GbE, 200 GbE, 100 GbE, 50 GbE, 40 GbE, 25 GbE, and 10 GbE operation. The supported FEC types include Clause-134 RS (544, 514), Clause-91 and Clause-108 RS (528, 514) RS-FEC, and FC (2212, 2080) FEC.

The device supports Auto-Negotiation and coefficient training protocol required by IEEE 802.3 to support operation over KR backplanes and CR passive copper cables. The device has a fully symmetric architecture with Long Reach SerDes, FEC generation and termination functionality, and Auto-Negotiation and training capabilities on both host and line interfaces for provide complete system design flexibility.

The 88X7121P also supports 2:1 multiplexing functionality with hitless switching capability on the host interface for applications requiring redundancy.

Block Diagram

16X56G PAM4/25G/10G/1G NRZ

Auto-Negotiation	Coefficient Training

Long Reach Host Interface

400GbE/200GbE/100GbE/50GbE/25GbE/10GbE/1GbE PCS + FEC

2:1 Mux with Hitless Switching

MAC+256 bit MACsec+PTP Time Stamping

400GbE/200GbE/100GbE/50GbE/25GbE/10GbE/1GbE PCS + FEC

MDIO	SyncE
JTAG	LED
Auto-Negotiation	Coefficient Training

56G-CR/KR Capable SerDes

16X56G PAM4/25G/10G/1G NRZ

Marvell 88X7121P Block Diagram

Key Features

Features	Benefits
Dual 400GbE, Quad 200GbE, Octal 100GbE, 16-port 50 GbE, 25 GbE, 10 GbE, 1 GbE MACsec with 256-bit key	· Enables encrypted links for all speeds from 1GbE up to 400GbE
Quad 100GbE gearbox for translation from IEEE 802.3bj 4x25G NRZ to IEEE 802.3cd 2x50G NRZ	· Enables support of 25G NRZ optics from switch ASICs with 50G PAM4 I/Os. Also enables support of new 50G-PAM4 optics with legacy switch ASICs
IEEE 1588v2 PTP Timestamping that meets timing accuracy requirements for Class C PTP profile	· Accurate extraction of timing information for timing critical applications
Recovered clock for SyncE applications with flexible selection of clock	· Enables accurate transfer of clock over Ethernet networks
2:1 Mux on the host interface with hitless switching	· For applications requiring Active/Standby redundancy with seamless switchover
Long Reach host and line interface SerDes	· For driving passive direct attach copper (DAC) cables and backplanes
Fully symmetric architecture with FEC capability on host and line interfaces	· Flexibility to support a wide range of applications and system design choices
Support for IEEE Auto Negotiation and Training protocol	· Seamless interoperability with standard-scompliant devices from other vendors
8x8 SerDes layer crossbar	· Enables board routing flexibility for the high speed I/Os
Ethernet packet and PRBS generation capabilities and eye monitoring capability on all high-speed interfaces	· Comprehensive test and debug capabilities

Target Applications

· 400G, 200G, 100G, 50G, 25G Datacenter switches
· 100G, 50G, 25G, 10G and 1G Enterprise and Carrier line cards